detected and fixed. Hardware problems include logic mistakes, incorrect circuit board connections, and improperly assembled systems. Regardless of its nature, a problem must be isolated before it can be corrected. Bugs can be hard to find in a digital system, because time is measured in nanoseconds, and logic 1s and 0s are not visually distinct as they flow across wires. The debugging process is made easier by employing specific design elements and methodologies that improve visibility into a system's inner workings.

A basic debugging aid is the ability to probe a digital circuit with an oscilloscope or logic analyzer so that the state of individual wires can be observed. (A logic analyzer is a tool that rapidly captures a set of digital signals and then displays them for inspection. Test equipment is discussed in more detail later on.) Some circuits require little or no modification to gain this visibility, depending on their density, packaging technology, and operating speed. A circuit that uses DIPs or PLCCs exclusively can be directly probed with an oscilloscope probe, and clip-on logic analyzer adapters may be used to capture many digital signals simultaneously. As circuits get denser and use fine-pitch surface mount ICs, it becomes necessary to use connectors specifically designed for logic analyzer attachment. The correct type of connector should be verified with your logic analyzer manufacturer. Using logic analyzer connectors provides access to a set of predetermined signals fairly rapidly, because a whole connector can be inserted or removed at one time rather than having to use individual clips for each signal.

Logic analyzer probing becomes more of a challenge at high frequencies because of transmission line effects. Top-of-the-line logic analyzers are designed to minimally load a bus, and they include controlled impedance connectors to reduce unwanted side effects of probing. Depending on the trace lengths involved and the specific ICs, minimal impact is possible with speeds around 100 MHz. Careful PCB layout is essential for these situations, and it is desirable to minimize stubs created by routing signals to the connectors. At frequencies above 100 MHz, transmission line effects can rapidly cause problems, and special impedance matching and terminating circuitry may be necessary to achieve nonintrusive logic analyzer probing. Logic analyzer manufacturers have circuit recommendations that are specifically customized to their products.

The ideal scenario is to have logic analyzer visibility for every signal in a system. In reality, 100 percent visibility is not practical. More complex buses are more difficult to debug and, consequently, stand to benefit more from logic analyzer connectors. A simple asynchronous microprocessor bus, on the other hand, can be debugged with an inexpensive analog oscilloscope if a logic analyzer is not available. Whereas logic analyzers stop time and display a timing diagram of the selected signals over a short span of time, analog oscilloscopes usually do not have this persistence. The persistence problem can be addressed with a technique known as a *scope loop*. A scope loop is usually implemented in software but can be done in hardware as well, and it performs the same simple operation continuously so that an oscilloscope can be used to observe what has become a periodic event.

Debugging a basic microprocessor bus problem with a scope loop can be explained with a brief example. Figure 19.8 shows a portion of a digital system in which a RAM is connected to a microprocessor and enabled with an address decoder. In normal operation, the microprocessor asserts an address that is recognized by the decoder, and the RAM is enabled. One possible bug is an incorrectly wired address decoder. If the microprocessor is unable to access the RAM, the first thing to check is whether the RAM's chip select is being asserted. A single RAM access cannot be effectively observed on a normal analog oscilloscope, because the event may last well under a microsecond. Instead, a scope loop can be created by programming the microprocessor to continually perform RAM reads. The chip select can now be observed on an oscilloscope, because it is a periodic event. If the chip select is not present, the address decoder's inputs and output can be tested one by one to ensure proper connectivity. If the chip select is being asserted, other signals such as output enable or individual address bits can be probed. Oscilloscopes have at least two channels, and the second channel can be used to probe one other signal in conjunction with chip select to observe rela-

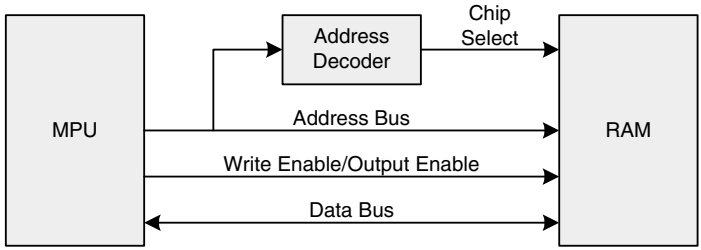

FIGURE 19.8 Microprocessor RAM interface.

tive timing. For example, if output enable is not asserted at the same time as chip select, the RAM will not respond to a read.

As a bus gets more complex, the two or four channels of a typical oscilloscope do not provide sufficient visibility into what is happening. This is where logic analyzers with dozens of channels are truly useful and why dedicated connectors are helpful in debugging digital systems.

Logic analyzer connectors alone can provide access to board-level signals only. Many digital systems implement logic within PLDs, with the result that many logic nodes are hidden from the board-level perspective. Proper simulation of a PLD can flush out many bugs, but others may escape detection until a real system is functioning in a lab environment. It is helpful to allocate unused pins on a PLD for test purposes so that internal nodes that are normally hidden can be driven out of the PLD and captured on a logic analyzer or oscilloscope.

19.6 BOUNDARY SCAN

When testing a newly fabricated system, there is generally the assumption of a properly wired and assembled circuit board. A high-quality manufacturing process should make this assumption realistic. The proliferation of BGA and very fine-pitch packaging has made PCB assembly a more delicate operation, because there is less room for error and less visibility to check for proper solder connections. BGAs are especially troublesome, because the solder ball connections are largely hidden from view. To make matters worse, a faulty BGA connection cannot simply be touched up in the lab with a soldering iron. The entire BGA must usually be removed from the board, cleaned, reprocessed, and then reattached. X-ray inspection machines are used to help verify proper BGA assembly, but these machines are imperfect and costly. If a prototype board initially arrives in the lab and fails to perform basic operations, the problem can be either assembly related or design related. This uncertainly lengthens the debugging process, because individual wires must be probed to verify connectivity because of the lack of visibility under a BGA package. Very fine-pitch leaded packages are also subject to inspection difficulty, because solder shorts can be hidden from view behind a screen of dense pins.

Members of the IEEE saw these assembly verification problems looming in the 1980s as packaging density continued to increase. The IEEE Joint Test Action Group (JTAG) was formed to address testability problems, and they developed the IEEE 1149.1 Standard Test Access Port and Boundary Scan Architecture. Because the full name of the standard is a mouthful, most people refer to IEEE 1149.1 simply as JTAG. JTAG is a simple yet powerful technology, because it places test resources directly into ICs and enables chaining multiple ICs together via a standard four- or five-wire serial interface. In essence, JTAG forms a long chain of shift registers whose contents can be set and read back through software. The placement of these shift registers, or test cells, determines the types of